

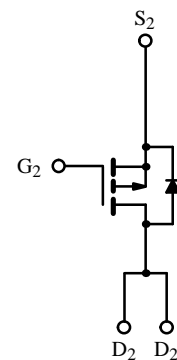
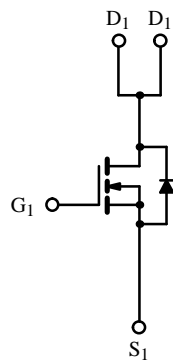
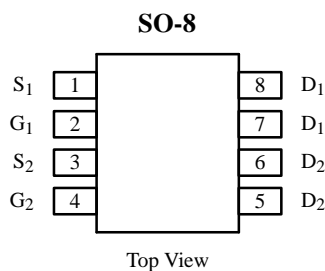
Dual Enhancement-Mode MOSFET (N- and P- Channel)

Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.10 @ V _{GS} = 10 V	± 3.5
		0.12 @ V _{GS} = 6 V	± 3
		0.15 @ V _{GS} = 4.5 V	± 2.5
P-Channel	-20	0.10 @ V _{GS} = -10 V	± 3.5
		0.12 @ V _{GS} = -6V	± 3
		0.19 @ V _{GS} = -4.5 V	± 2.5

Recommended upgrade: Si4532DY or Si4539DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6543DQ



Absolute Maximum Ratings (T_A = 25° C Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150° C) ^a	I _D	T _A = 25° C	± 3.5	A
		T _A = 70° C	± 2.8	
Pulsed Drain Current	I _{DM}	± 14	± 14	A
Continuous Source Current (Diode Conduction) ^a	I _S	1.7	-1.7	
Maximum Power Dissipation ^a	P _D	T _A = 25° C	2.0	W
		T _A = 70° C	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1223. A SPICE Model data sheet is available for this product (FaxBack document #5115).

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

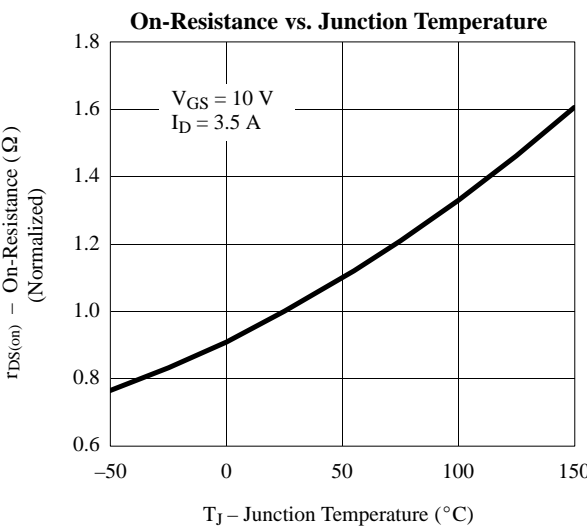
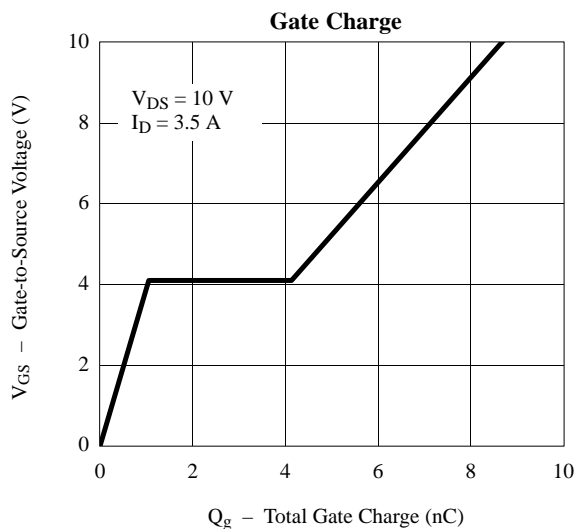
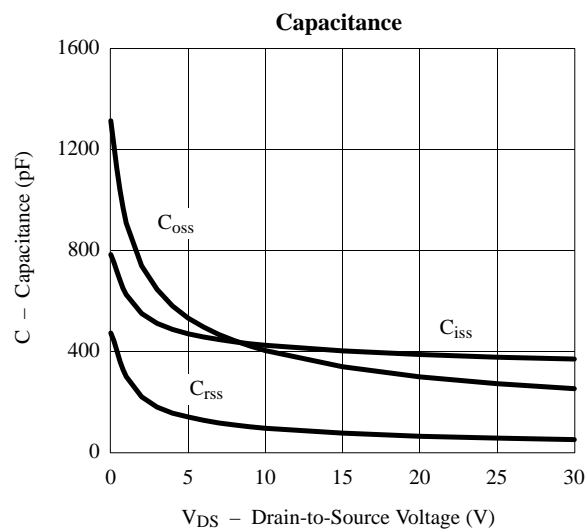
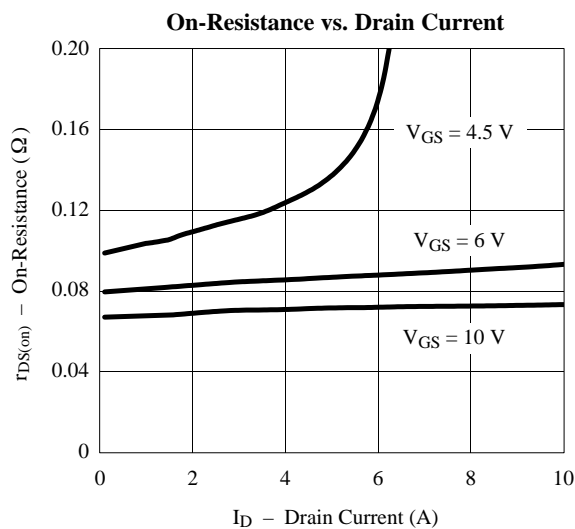
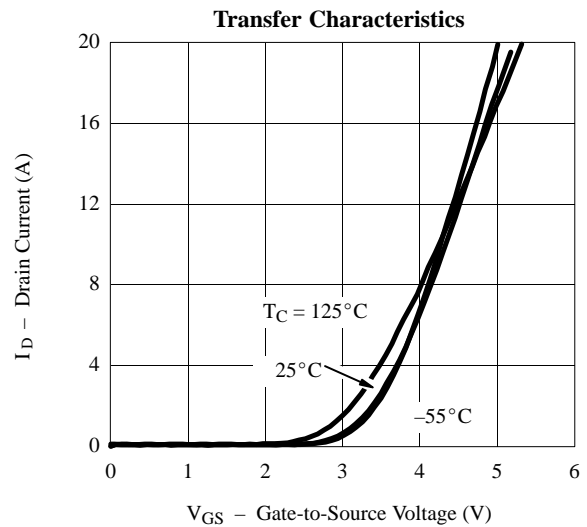
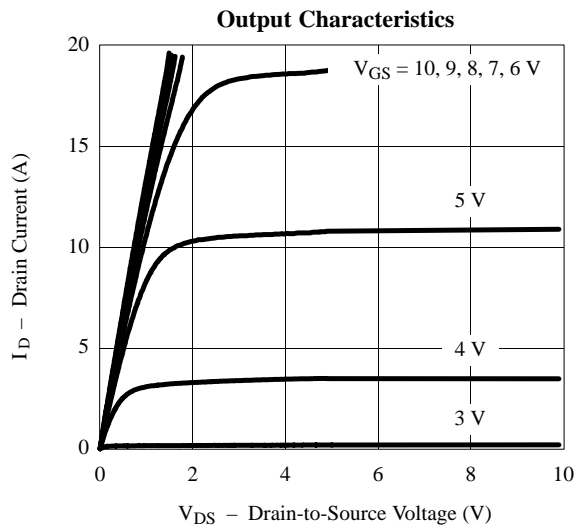
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1.0		V
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	-1.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$	N-Ch		1	μA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$	P-Ch		-1	
		$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$	N-Ch		5	
		$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 70^\circ\text{C}$	P-Ch		-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	N-Ch	14		A
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -10 \text{ V}$	P-Ch	-14		
		$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	N-Ch	3.5		
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	P-Ch	-2.5		
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$	N-Ch		0.10	Ω
		$V_{GS} = -10 \text{ V}, I_D = 3.5 \text{ A}$	P-Ch	0.05	0.10	
		$V_{GS} = 6 \text{ V}, I_D = 3 \text{ A}$	N-Ch		0.12	
		$V_{GS} = -6 \text{ V}, I_D = 3 \text{ A}$	P-Ch	0.08	0.12	
		$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$	N-Ch		0.15	
		$V_{GS} = -4.5 \text{ V}, I_D = 2 \text{ A}$	P-Ch		0.19	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 3.5 \text{ A}$	N-Ch		5.6	S
		$V_{DS} = -15 \text{ V}, I_D = -3.5 \text{ A}$	P-Ch		4.0	
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch		0.9	V
		$I_S = -1.7 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch		-0.9	
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$ $V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -3.5 \text{ A}$	N-Ch		9	nC
Gate-Source Charge	Q_{gs}		P-Ch		13	
			N-Ch		1.0	
Gate-Drain Charge	Q_{gd}		P-Ch		2.0	
		N-Ch		3.1		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$ $V_{DD} = -10 \text{ V}, R_L = 10 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 6 \Omega$	N-Ch		5	ns
			P-Ch		21	
Rise Time	t_r		N-Ch		12	
			P-Ch		12	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		17	
			P-Ch		12	
Fall Time	t_f		N-Ch		9	
			P-Ch		11	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	N-Ch		60	100
			P-Ch		50	

Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

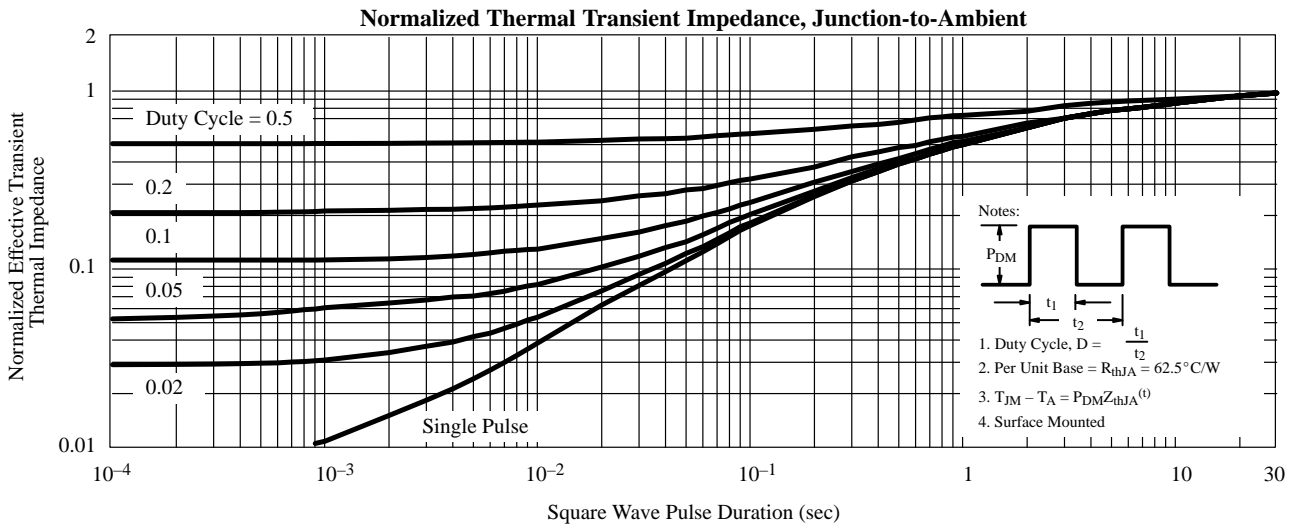
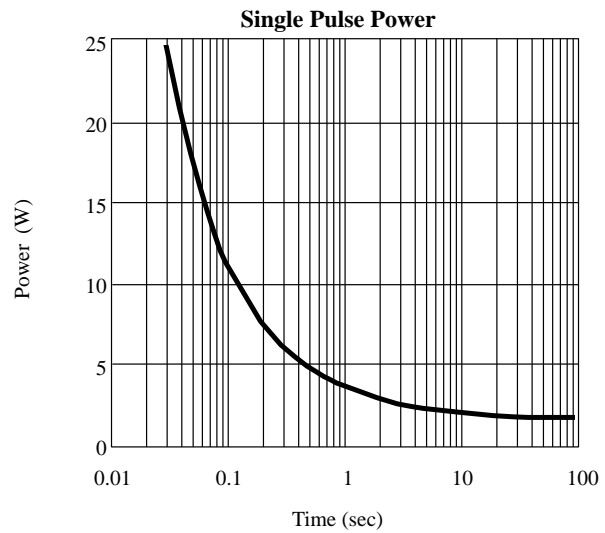
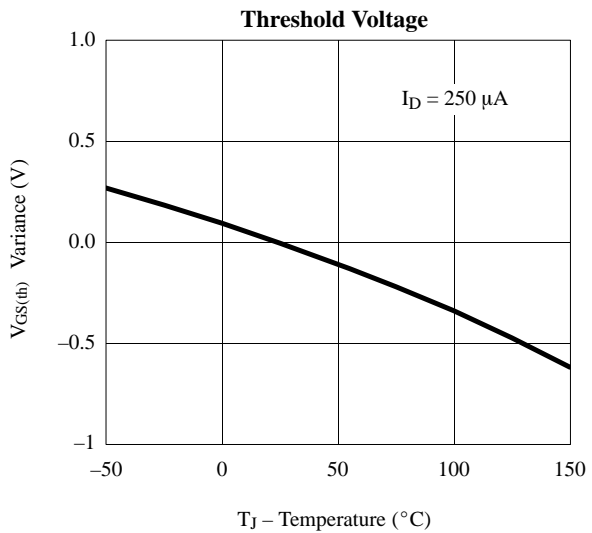
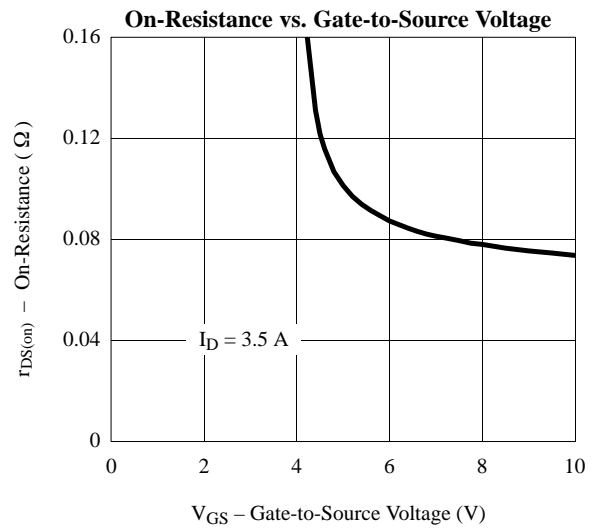
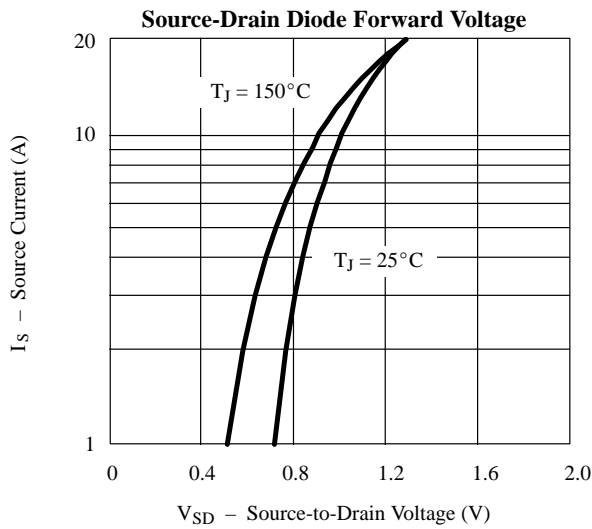
Typical Characteristics (25°C Unless Otherwise Noted)

N-Channel



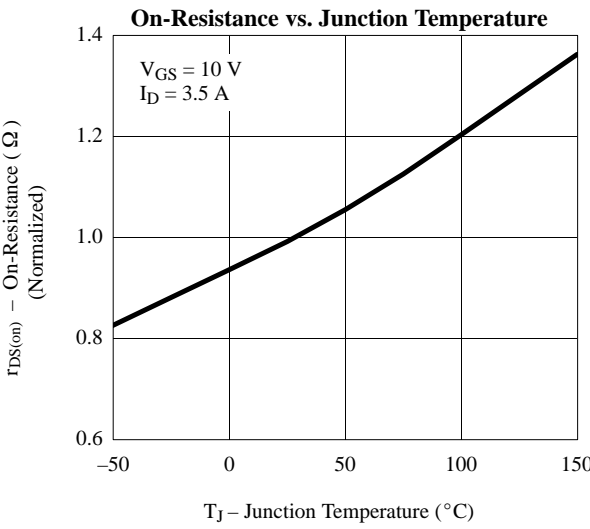
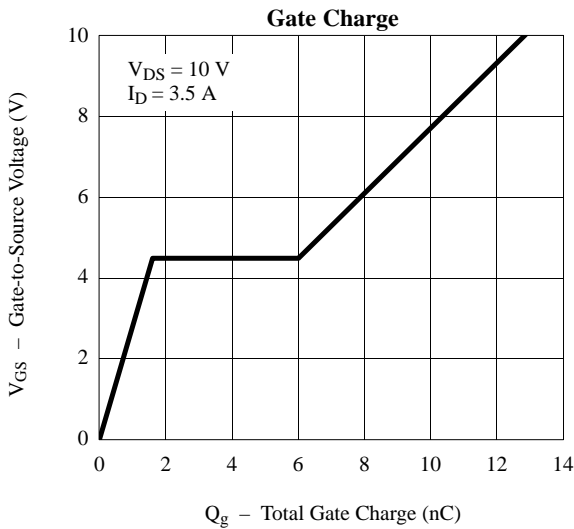
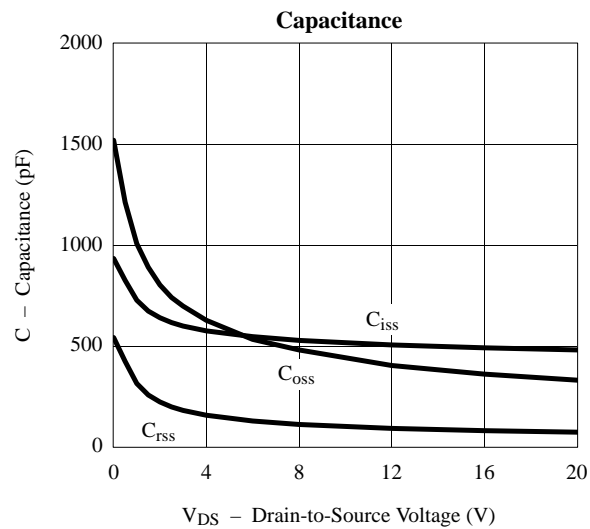
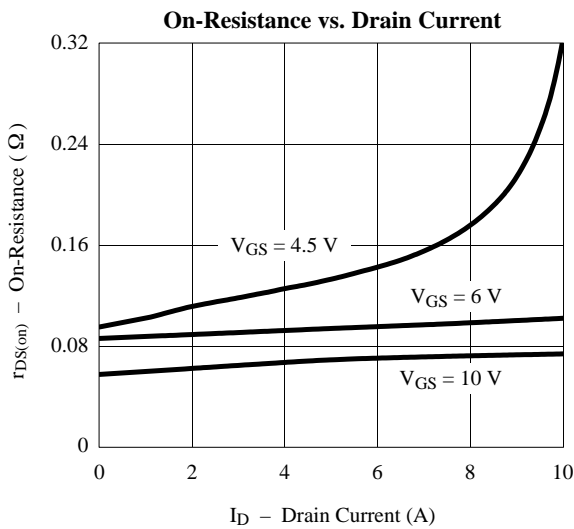
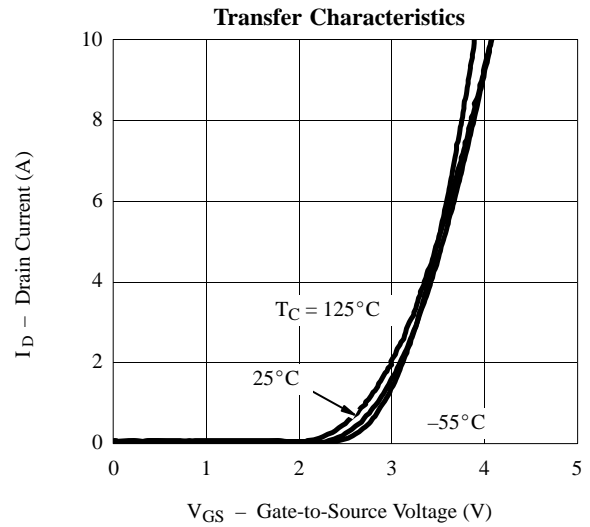
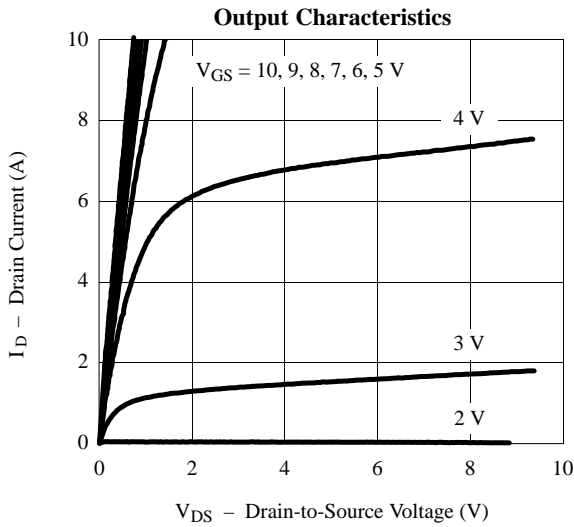
Typical Characteristics (25°C Unless Otherwise Noted)

N-Channel



Typical Characteristics (25°C Unless Otherwise Noted)

P-Channel



Typical Characteristics (25°C Unless Otherwise Noted)

P-Channel

